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	Application Number	10/025,289
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	First Named Inventor	Andrew K. Martin et al.
	Group Art Unit	2825
	Examiner Name	Annette M. Thompson
Total Number of Pages in this Submission	Attorney Docket Number	SC11522TS

ENCLOSURES (check all that apply)

☐ Fee Transmittal Form	☐ Assignment Papers (for an Application)	☐ After Allowance Communication to Group
☐ Fee Attached	☐ Drawing(s)	☐ Appeal Communication to Board of Appeals and Interferences
☐ Amendment/Reply	☐ Licensing-Related papers	X Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
☐ After Final	☐ Petition	☐ Proprietary Information
☐ Affidavits/Declaration(s)	☐ Petition to Convert to a Provisional Application	☐ Status Letter with appropriate copies
☐ Extension of time Request	☐ Power of Attorney, Revocation, Change of Correspondence Address	X Other Enclosure(s) (please identify below) ☒ Response to Notice of Non-Compliance with 37 CFR 1.192(c) ☒ Return Postal Card ☐ RCE
☐ Express Abandonment Request		
☐ Information Disclosure Statement	☐ Terminal Disclaimer	
☐ Certified Copy of Priority Documents	☐ Request for Refund	
☐ Response to Missing Parts/ Incomplete Application	☐ CD, Number of CDs	
☐ Response to Missing Parts Under 37 CFR 1.52 or 1.53	Remarks	

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Date	11/29/04		

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DOCKET NO. SC11522TS

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S)	Andrew K. Martin et al.	GROUP ART UNIT:	2825
APPLN. NO.:	10/025,289	EXAMINER:	Annette M. Thompson
FILED:	December 19, 2001		
TITLE:	DESIGN VERIFICATION SYSTEM FOR AVOIDING FALSE FAILURES AND METHOD THEREFOR		

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Date of deposit: 11-29-04
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RESPONSE TO NOTICE OF NON-COMPLIANCE WITH 37 CFR 1.192(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the Office Action dated October 28, 2004, Applicant is submitting a corrected Brief on Appeal in triplicate.

It is believed that no fees are due, however if Applicant has overlooked any additional fees, the Commissioner is hereby authorized to debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

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Law Department

Customer Number: 23125

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Andrew K. Martin et al.
Serial No.: 10/025289
Filed: December 19, 2001
For: DESIGN VERIFICATION SYSTEM FAILURES AND METHOD THEREFOR

Date Originally Submitted:
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Art Unit: 2825
Examiner: Annett M. Thompson
Docket No.: SC11522TS

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:
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APPELLANTS' BRIEF ON APPEAL

COMMISSIONER OF PATENTS AND TRADEMARKS
ALEXANDRIA, VA 22313-1450

BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed pursuant to 37 C.F.R. §1.192 in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent. Authorization to charge Appellants' deposit account for fees associated with filing this Appeal Brief is provided in an accompanying Fee Transmittal paper.

REAL PARTY IN INTEREST

The present application is wholly assigned to FREESCALE SEMICONDUCTOR, INC., a Delaware corporation with its headquarters in Austin, Texas.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-26 are the subject of this appeal. Claims 1-26 were presented to the USPTO for the first time on December 19, 2001, the filing date of the present application. In a first Office Action, the Examiner objected to claims 9 and 16, rejected claims 1-18 and 21-25 under 35 USC 102 (e) as being anticipated by Martin et al. (US Patent 6,378,112), rejected claims 19, 20, and 26 under 35 USC 102(b) as being anticipated by Pixley et al. (US Patent 5,754,454). Appellants responded to the objection by amending claims 9 and 16, and responded to the rejection of claims 1-26 with arguments. The Examiner finally rejected the claims on the same grounds as originally rejected, and withdrew the objections of claims 9 and 16. Appellants responded in an after final response with arguments. At this point, claims 1-26 were still pending. The Examiner did not find Appellants' arguments persuasive. Thus, Appellants submitted a Notice of Appeal on June 3, 2004. This Appeal Brief is being submitted in support of the Notice of Appeal.

STATUS OF AMENDMENTS

The claims being appealed are claims 1-8, 10-15, and 17-26 as originally filed, and claims 9 and 16 as amended in Appellants' reply submitted November 21, 2003.

SUMMARY OF THE INVENTION

A verification system, such as that illustrated in FIG. 1, may use Symbolic Trajectory Evaluation (STE) to compare one design representation such as a reference model, with another representation of the same design (or of a different design) such as an implementation model. STE allows for increased coverage when some values are allowed to be "unknown" rather than a logic low or logic high. However, the use of STE may result in false failures. Therefore, one aspect of the present invention provides for comparing an expected result from the reference design to an actual result of the implementation design in order to determine a set of failure conditions. Constraints are then selectively applied to the set of failure conditions in an attempt to remove them. Another aspect of the present invention allows for the selective use of symbols rather than unknowns in order to avoid false failures due to certain inputs of the implementation design not being properly simulated.

FIG. 1 illustrates one embodiment of a verification system 101 which operates to compare a functionality of implementation design 104 with a predetermined functionality of reference design 102. That is, it is not necessary for reference design 102 and implementation design 104 to be fully functionally equivalent. However, implementation design 104 may introduce variable dependencies that are not apparent in reference design 102, thus leading to the detection of false failures. Verification system 101 therefore provides for avoiding false failures.

Reference design 102 is input to a symbolic assertion generator 108. Symbolic assertion generator 108 also receives design inputs 106. Design inputs 106 include clock phase-based timing types for primary inputs, latches, primary outputs, and bit cells of memory arrays. Design inputs 106 may also include user specified constraints for use by symbolic assertion generator 108 and symbolic simulator 110. Design inputs 106 may also include additional reference design nodes which may either be user specified or tester generated (i.e. generated by symbolic assertion generator 108 or symbolic simulator 110). Symbolic assertion generator 108 produces assertions 112 from reference design 102 and design inputs 106. Assertions 112 are used to provide stimulus and expected results for symbolic simulation. Assertions 112 are fed into symbolic simulator 110 that also receives data for implementation design 104. Symbolic simulator 110 also receives constraints 116. These constraints may include implicit constraints (those generated by symbolic assertion generator 108) or user specified constraints (e.g. those that are explicitly stated by a user of verification system 101 and provided as part of design inputs 106).

FIG. 4 illustrates a method of comparing different views of a circuit design, according to one embodiment of the present invention. The flow of Fig. 4 is described in detail on pages 9-15, using reference design 200 of FIG. 2 and implementation design 300 of FIG. 3 as an example, and the flow of FIG. 8, which further describes block 406 of FIG. 4, is described in detail on pages 19-20. The flow of FIG. 4 describes, for example, obtaining assertions 112 (which, as described in FIG. 8, may include the use of user specified additional reference design nodes), obtaining a failure condition, obtaining a set of constraints, and applying one or more constraints from the set of constraints to the failure condition to try and remove the failure condition.

If the failure condition is not removed with the application of all the constraints available (i.e. upon reaching block 436 of FIG. 4), the design inputs can optionally be modified to take care of the failure condition. For example, if it is suspected that the failure condition is actually a false failure condition, a user or a tester can analyze the failure condition and specify additional reference design nodes for stimulation in order to avoid false failures. For example, these additional nodes may result from the fact that

the actual circuit design (such as the implementation design) may include a dependency that was not apparent in the reference design. The addition of these nodes is discussed in reference to FIGs. 7 and 8. For example, in FIG. 7, nodes a 722 and b 724 are specified in order to ensure that these nodes receive proper stimulus.

ISSUES

1) Are claims 1-18 and 21-25 anticipated by Martin et al. (US 6,378,112), under 35 U.S.C. 102(e)?
2) Are claims 19, 20, and 26 anticipated by Pixley et al. (US 5,754,454), under 35 U.S.C. 102(b)?

GROUPING OF CLAIMS

Group A → Claims 1-9, 12-16, and 18
Group B → Claims 10 and 11
Group C → Claim 17
Group D → Claims 19 and 20
Group E → Claims 21, 22, 24, and 25
Group F → Claim 23
Group G → Claim 26

The requested division is on the basis that the claims of Group A are directed to a verification system or a method for verifying functional similarity between a first design and a second design which includes applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring. The claims of Group A are rejected over Martin et al., and they stand or fall together. The claims of Groups B and C are dependent off of Group A, but include additional limitations. The claims of Group B stand or fall together. The claims of Group D are directed to a

computer readable storage medium for storing a verification system which includes a set of instructions which, when executed, implement a process including applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring. The claims of Group D are rejected over Pixley et al., and they stand or fall together. The claims of Group E are directed to a verification system or a method of verifying functional similarity between a first design and a second design which includes analyzing the representation of the first design to determine a set of inputs to a test point, generating a set of symbolic stimulus to be applied to the corresponding test point inputs in the representation of the second design, accepting as an additional input one or more additional nodes in the first design, finding additional inputs in the first design corresponding to the additional nodes, generating a second set of symbolic stimulus from the additional inputs, applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design, and generating an output response for use in verifying functional similarity. The claims of Group E are rejected over Martin et al., and they stand or fall together. The claim of Group F is dependent off of Group E, but includes additional limitations. The claim of Group G is directed to a computer readable medium for storing a verification system which includes a set of instructions which, when executed, implement a process including analyzing the representation of the first design to determine a set of inputs to a test point, generating a set of symbolic stimulus to be applied to the corresponding test point inputs in the representation of the second design, accepting as an additional input one or more additional nodes in the first design, finding additional inputs in the first design corresponding to the additional nodes, generating a second set of symbolic stimulus from the additional inputs, applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design, and generating an output response for use in verifying functional similarity. The claim of Group G is rejected over Pixley et al.

ARGUMENTS

Arguments Common to Groups A, B, and C

The Examiner uses Martin in the rejections of claims 1-18 (of Groups A, B, and C) under 35 U.S.C. 102(e). In regards to the rejections using Martin under 35 U.S.C. 102(e), Appellants respectfully submit that claims 1-18 are not anticipated by the cited prior art. A reference is anticipatory only if it discloses all limitations of a claim. *Jamesbury Corp. v. Litton Indus. Products*, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); *Atlas Powder Co. v. du Pont*, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984).

More specifically, with respect to independent claims 1 and 13, Appellants submit that Martin does not teach each and every element recited in claims 1 and 13. Each of claims 1 and 13 include providing a failure indicator and a characterization of a failure, applying one or more constraints to the characterization of the failure, the one or more constraints representing restriction on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring. In the Office Action mailed August 21, 2003, the Examiner states that these elements of claims 1 and 13 are taught by Martin and cites col. 6, ll. 11-11 [sic], of Martin (which Appellants assume refers to col. 6, ll. 1-11 of Martin because lines 1-11 were underlined by the Examiner in the copy of the patent that Appellants received and these lines were again cited in the Final Office Action mailed March 3, 2004). However, this cited section simply discusses the ability to test and debug a design block more quickly, but this does not teach the elements of claim 1 or claim 13 cited above, such as the use of failure indicators and characterizations of a failure or the use of constraints as claimed in each of claims 1 and 13. Furthermore, nothing else in col. 6, or the remainder of Martin teaches these elements.

In the Remarks section of the Final Office Action mailed March 3, 2004, the Examiner states that the elements of applying one or more constraints .... (referring to claim 1), are taught by the tester in Martin (FIG. 2, #208, 210) and by the text in col. 6, lines 1-16. However, these sections of Martin do not teach the elements of applying one

or more constraints to the characterization of the failure, the one or more constraints representing restriction on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring. In this Remarks section, the Examiner states that Martin discloses "the use of an identity match (col. 6, ll. 5-13) and a characterization of the failure (col. 6, ll. 16-18)." However, col. 6, ll. 5-13, does not disclose the use of an identity match, and col. 6, ll. 16-18, does not disclose a characterization of the failure. Furthermore, even if it is assumed that Martin discloses an identity match (which the Examiner maps to the element of a failure indicator in claim 1) and a characterization of the failure, nothing in these cited sections of col. 6, nor in the remainder of Martin, teach the further details of applying one or more constraints to the characterization of the failure, the one or more constraints representing restriction on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring.

Therefore, as described above, the elements of claim 1 (and claim 13) are directed to a novel verification system/method, different from the one disclosed in Martin. While Martin and the current Application both address a tool for verifying two designs, the current Application recognizes and addresses problems that are not discussed or addressed in Martin. For example, the existence of false failures caused through the use of symbolic simulation (as described in the current Application) is not addressed in Martin. While some of the drawings and text are similar in Martin and the current Application, the methodology for verifying two designs is different in each. For example, the methodology illustrated in the flow diagram of FIG. 4 in the current Application, which supports many of the novel elements discussed above in claims 1 and 13, is not taught or even present in Martin, which uses a completely different methodology, e.g. see FIGs. 3 and 4 of Martin. Appellants also wish to point out that under 35 U.S.C. 103(c), Martin cannot be used in a 103(a) (i.e. obviousness) rejection against the current claims because the current Application and Martin were commonly assigned to Motorola, Inc, at the time of invention.

For at least these reasons, independent claims 1 and 13 and dependent claims 2-12 and 14-18 are patentable over Martin under 35 U. S.C. 102(e), and reversal is respectfully requested.

Additional Arguments for Group B

The Examiner also uses Martin in the rejections of claims 10 and 11 of Group B. As stated above, claims 10 and 11 depend from claim 1 and are therefore, at least allowable for those reasons provided above with respect to claim 1. Claim 10, dependent from claim 1, further claims wherein the one or more constraints comprise a set of constraints, and an order in which the set of constraints is applied is dependent upon the characterization of the failure. Martin also does not teach or suggest these elements. Firstly, as state above, Martin does not teach constraints (representing restrictions on permissible test parameter of the second design representation) as claimed in claims 1 and 10. Secondly, Martin does not teach that an order of applying a set of constraints is dependent upon the characterization of the failure. The Examiner, in the Office Action mailed August 21, 2003, states that the elements of claim 10 are taught by Martin in col. 5, ll. 41-67. This section simply discusses an example of data produced by step 306 of FIG. 3 in which stable schematic time intervals are assigned for latches, primary inputs, outputs and cutpoints. This example data is illustrated in FIG. 7 in a digital wave form diagram in FIG. 7 to illustrated the timing of signals. However, neither this section nor any of the remaining sections of Martin teach the additional elements of claim 10. Claim 11 depends from claim 10 and is therefore allowable for those reasons stated above with respect to claim 1 and for the additional reasons stated herein with respect to claim 10.

Therefore, for these additional reasons, Appellants respectfully submit that the claims of Group B are allowable. Reversal is respectfully requested.

Additional Arguments for Group C

The Examiner also uses Martin in the rejections of claim 17 of Group C. As stated above, claim 17 depends from claim 13 and is therefore, at least allowable for those reasons provided above with respect to claim 13. Claim 17 further claims creating a set of constraints, and applying predetermined ones of the set of constraints in an order that is dependent upon the characterization of the failure. Martin also does not teach or suggest these elements. Firstly, as state above, Martin does not teach constraints (representing restrictions on permissible test parameter of the second design representation) as claimed in claims 13 and 17. Secondly, Martin does not teach that an order of applying a set of constraints is dependent upon the characterization of the failure. The Examiner, in the Office Action mailed August 21, 2003, states that the elements of claim 17 are taught by Martin in col. 5, ll. 41-67. This section simply discusses an example of data produced by step 306 of FIG. 3 in which stable schematic time intervals are assigned for latches, primary inputs, outputs and cutpoints. This example data is illustrated in FIG. 7 in a digital wave form diagram to illustrate the timing of signals. However, neither this section nor any of the remaining sections of Martin teach the additional elements of claim 17.

Therefore, for these additional reasons, Appellants respectfully submit that the claims of Group C are allowable. Reversal is respectfully requested.

Arguments for Group D

The Examiner uses Pixley in the rejections of claims 19 and 20 of Group D under 35 U.S.C. 102(b). In regards to the rejections using Pixley under 35 U.S.C. 102(b), Appellants respectfully submit that claims 19 and 20 are not anticipated by the cited prior art. A reference is anticipatory only if it discloses all limitations of a claim. *Jamesbury Corp. v. Litton Indus. Products*, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); *Atlas Powder Co. v. du Pont*, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984).

More specifically, with respect to independent claim 19, Appellants submit that Pixley does not teach each and every element recited in claims 19. Claim 19 includes a computer readable storage medium for storing a verification system having a set of instructions, which, when executed, implement a processing including comparing a representation of a second design with a representation of a first design, providing a failure indicator and a characterization of a failure, applying one or more constraints to the characterization of the failure, the one ore more constraints representing restrictions on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring. In the Office Action mailed August 21, 2003, the Examiner states that these elements are taught by Pixley and cites col. 5, ll. 38-57. However, this cited section simply discusses the screening out of invalid cutpoint pairs, but this does not teach the elements of claim 19 cited above, such as the use of failure indicators and characterizations of a failure or the use of constraints. Furthermore, the removal of invalid cutpoint pairs is not relevant to these elements of claim 19. For example, the removal of invalid cutpoints using the ATPG techniques of Pixley may be done in addition to the claimed elements of claim 19 cited above or may not be done at all.

In the Remarks section on page 9 of the Final Office Action mailed March 3, 2004, the Examiner states that "Pixley's cutpoint variables represent constraints which are substituted into an XOR model to determine a failure condition, column 6, lines 25-40," and that "Variables (constraints) are substituted and it is determined which variables result in failure." However, Appellants respectfully submit that the Examiner has mischaracterized the variables of Pixley. Firstly, in claim 19, the constraints are applied to determine if they will *prevent* a previously detected failure from occurring. Secondly, the cutpoint variables of Pixley are not constraints *which represent restrictions on permissible test parameters*. In Pixley, when a cutpoint does not result in a match (the output of the XOR is not a one or a zero), the cutpoint is replaced with its actual function. For example, referring to FIG. 8 of Pixley, the use of cutpoint variable X results in XOR_OUT being 1 for B=0 and X=1, but being 0 for the remainder of the inputs. Therefore, this cutpoint is not a valid cutpoint and is completely removed and therefore replaced with its actual function ("A or B" as seen in FIG. 5 of Pixley). Thus,

cutpoint variable X is no longer present. However, cutpoint variable X is NOT a constraint which restricts permissible test parameters. That is, when cutpoint variable X is present (e.g., when it is valid), it can be any value *without restriction*. However, if it is invalid, it is removed all together (e.g. replaced with its actual function) and is therefore also not used to restrict permissible test parameters because it no longer affects the XOR circuit at all. Instead, variables A and B are used, where A and B can be any value, without restriction.

As described in the current Application, cutpoints may be used to *generate* constraints (see, for example, page 8, line 27, through page 9, lines 8). For example, on these pages, cutpoint R216 (in FIG. 2) is introduced, where R and S are still inputs (to, e.g., gates 202 and 204, respectively, of FIG. 2); however, cutpoint R216 is used to obtain a constraint of "R= NOT S" which restricts permissible test parameters for R and S. In Pixley, if cutpoint variable X is present, no restrictions are provided for X, and if it is removed and thus replaced by its actual function, it is no longer a test parameter. Therefore, the cutpoint variables of Pixley do not teach or suggest the constraints as claimed in claim 19.

For at least these reasons, Appellants submit that claim 19 is allowable over Pixley. Claim 20, which depends from claim 19, is therefore also allowable for at least those reasons stated above with respect to claim 19. Reversal is respectfully requested.

Arguments Common to Groups E and F

The Examiner uses Martin in the rejections of claims 21-25 (of Groups E and F) under 35 U.S.C. 102(e). In regards to the rejections using Martin under 35 U.S.C. 102(e), Appellants respectfully submit that claims 21-25 are not anticipated by the cited prior art. A reference is anticipatory only if it discloses all limitations of a claim. *Jamesbury Corp. v. Litton Indus. Products*, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); *Atlas Powder Co. v. du Pont*, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984).

More specifically, with respect to independent claims 21 and 24, Appellants submit that Martin does not or suggest each and every element recited in claims 21 and

24. Each of claims 21 and 24 include analyzing with a symbolic stimulus generator the representation of the first design to determine a set of inputs to a test point, generating a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design, accepting as an additional input one or more additional nodes in the first design, finding additional inputs in the first design corresponding to the additional nodes, generating a second set of symbolic stimulus from the addition inputs, and applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design and generating an output response for use in verifying functional similarity. In the Office Action mailed August 21, 2003, the Examiner states that the elements of claim 21 are taught by Martin at FIG. 2, #210; col. 2, lines 63 to col. 3, lines 67. However, FIG. 2 and the cited sections of Martin (col. 2, line 63 to col. 3, line 67) clearly do not teach these elements. Martin describes a symbolic assertion generator and a symbolic simulator which do not take into consideration the use of additional nodes as claimed in claims 21 and 24 which may, for example, be used to address the issue of false failures. For example, note that the inputs to symbolic assertion generation 208 of FIG. 2 in Martin include only design inputs while the inputs to symbolic assertion generation 108 of the current Application includes design inputs as well as additional reference design nodes. Therefore, for at least these reasons, Applicants submit that claims 21 and 24 are clearly not anticipated by Martin.

In the Remarks section on page 8 of the Final Office Action mailed March 3, 2004, the Examiner states "Independent claims 21 and 24 recite this limitation [of additional nodes] and it is disclosed in Martin at fig. 2, #206 which **necessarily** includes additional nodes, (cf. Applicants' Fig. 1, #106, the parenthetical information)" (emphasis added). However, Appellants submit that this response is improper. The Examiner cannot use sections of Appellants' own specification (which are NOT indicated as being prior art) to reject the claims. That is, the reason that fig. 2, #206 of Martin did not include the additional nodes is because Martin does not teach or suggest them at all. That is, the design inputs of Martin at fig. 2, #206 ***do not necessarily include additional nodes***, as asserted by the Examiner. (See, for example, col. 2, line 60-62, of Martin which never even mentions the additional nodes while the current Application on, for

example, page 6, lines 4-8, clearly includes additional nodes in the design inputs). The use of additional nodes in avoiding false failures is an aspect of the current Application (and **not** of Martin) and was thus included into FIG. 1, #106 of the current Application and also provides one of the novel aspects of claims 21 and 24. The Examiner therefore cannot use FIG. 1, #106 of the current application to conclude that this type of design input is known.

Appellants provided the response described in the previous paragraph to the Examiner in a Response to Final Office Action mailed May 3, 2004. The Examiner, in the Advisory Action mailed May 25, 2004, in an attempt to respond to Appellants response with respect to claims 21 and 24, states "contrary to Applicants' assertion, the instant rejections are not based on Applicants' disclosure," and proceeds to state "Cf., shorthand for the word 'compare', was referenced in the Remarks section of the final rejection and is not relied on for the substantive rejection therein." Appellants disagree with this comment made by the Examiner. Appellants originally argued why Martin does not teach, for example, additional nodes. In response to Appellants Arguments (i.e. in the Remarks section of the Final Office Action), the Examiner states that Martin at fig. 2, #206 **necessarily** includes additional nodes. In doing so, the Examiner "compares" Martin's FIG. 2, #206 with Appellants' FIG. 1, #106 (the parenthetical information) to show that design inputs necessarily include additional nodes. Therefore, Appellants reasonably construe this statement by the Examiner as the Examiner using the specification of the current Application to reject claims 21 and 24 in the current Application. However, Appellants submit that this is improper. Also, Appellants wish to note that simply because FIG. 2 of Martin may appear similar to FIG. 1 of the current Application, many elements and details are included with respect to FIG. 1 of the current Application and described throughout the text of the current Application which differentiate FIG. 1 of the current Application from FIG. 2 of Martin. That is, as was mentioned above, Martin and the current Application provide different methodologies for verifying two designs, where the claims of the current Application, such as claims 21 and 24, are directed to aspects which are not taught or even discussed by Martin.

Appellants also wish to point out that under 35 U.S.C. 103(c), Martin cannot be used in a 103(a) (i.e. obviousness) rejection against the current claims because the

Application and Martin were commonly assigned to Motorola, Inc., at the time of invention.

Therefore, for at least these reasons, independent claims 21 and 24 and dependent claims 22-23 and 25 are patentable over Martin under 35 U. S.C. 102(e), and reversal is respectfully requested.

Additional Arguments for Group F

The Examiner also uses Martin in the rejection of claim 23 of Group F. As stated above, claim 23 depends from claim 21 and is therefore at least allowable for those reasons provided above with respect to claim 21. Claim 23 further claims wherein the corresponding inputs in the representation of the second design do not structurally exist in identical form in the representation of the first design, but correspondence in functional result exists. Martin also does not teach or suggest these elements. Unlike in Martin, the inputs of the two designs being verified need not match exactly. For example, additional nodes may be used in the current Application to help identify and address false failures, where, as described above, Martin does not discuss the use of additional nodes. The Examiner, in the Office Action mailed August 21, 2003, states that the elements of claim 23 are taught by Martin in col. 2, ll. 15-43. This section describes the design views of FIG. 2 but makes no mention as to whether the inputs can be non-identical. Furthermore, this section, nor the rest of Martin, discuss the possibility of additional nodes or varied inputs. That is, Martin is silent as to the elements of claim 23.

Therefore, for these additional reasons, Appellants respectfully submit that the claims of Group F are allowable. Reversal is respectfully requested.

Arguments for Group G

The Examiner uses Pixley in the rejections of claim 26 of Group G under 35 U.S.C. 102(b). In regards to the rejections using Pixley under 35 U.S.C. 102(b), Appellants respectfully submit that claim 26 is not anticipated by the cited prior art. A

reference is anticipatory only if it discloses all limitations of a claim. *Jamesbury Corp. v. Litton Indus. Products*, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); *Atlas Powder Co. v. du Pont*, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984).

More specifically, with respect to independent claim 26, Appellants submit that Pixley does not or suggest each and every element recited in claims 26. Claim 26 includes a computer readable storage medium for storing a verification system having a set of instructions, which, when executed, implement a process including analyzing with a symbolic stimulus generator the representation of the first design to determine a set of inputs to a test point, generating a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design, accepting as an additional input one or more additional nodes in the first design, finding additional inputs in the first design corresponding to the additional nodes, generating a second set of symbolic stimulus from the addition inputs, and applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design and generating an output response for use in verifying functional similarity. The Examiner, in the Office Action mailed August 21, 2003, states that claim 26 incorporates limitations already rejected by claim 19 and states that the BDD creations of Pixley (in col. 2, ll. 35-57) teaches the limitation of a symbolic stimulus generator. Firstly, the elements of claim 26 do not merely incorporate limitations present within claim 19. That is, many elements of claim 26 do not appear in claim 19, and the Examiner did not point out where each of these elements are found in disclosed in Pixley. Regardless, though, Appellants submit that Pixley does not teach or suggest each and every element of claim 26. Furthermore, claim 26 does not simply claim generating a set of symbolic stimulus. For example, as stated above, claim 26 claims accepting as an additional input one or more additional nodes in the first design, finding additional inputs in the first design corresponding to the additional nodes, generating a second set of symbolic stimulus from the addition inputs, and applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design and generating an output response for use in verifying functional similarity. These elements are not taught or

suggested by the BDD creations of Pixley (such as those described in col. 2, lines 35-57).

Therefore, for at least these reasons, Appellants respectfully submits that the claim of Group G is allowable. Reversal is respectfully requested.

Respectfully submitted,

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APPENDIX

1. A verification system comprising:

a representation of a first design representing a specification having a predetermined functionality;

a representation of a second design, the representation of the second design intended to satisfy the predetermined functionality of the first design, the verification system functioning to affirm that the representation of the second design satisfies the predetermined functionality of the representation of the first design;

a plurality of design inputs;

a tester for comparing the representation of the second design with the representation of the first design, and detecting when the representation of the second design does not satisfy the representation of the first design, the tester providing a failure indicator and a characterization of a failure in response to the detecting, the tester further comprising:

a failure analyzer for applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring.

2. The verification system of claim 1 wherein the verification system functions to affirm that the second design is fully functionally equivalent to the first design.

3. The verification system of claim 1 wherein one of the first design or the second design is an RTL representation and the other is a gate level representation.

4. The verification system of claim 1 wherein one of the first design or the second design is an RTL representation and the other is a transistor level representation.

5. The verification system of claim 1 wherein the representation of the first design and the representation of the second design are two different representations of a same design.

6. The verification system of claim 1 wherein the constraints are supplied as design inputs.

7. The verification system of claim 1 wherein the constraints are supplied by a user of the verification system.

8. The verification system of claim 1 wherein the constraints originate from the tester.

9. The verification system of claim 1 wherein the first design and the second design represent a portion of an integrated circuit design that is less than all of the integrated circuit design, and wherein another portion of the integrated circuit design at least partially determines the one or more constraints.

10. The verification system of claim 1 wherein the one or more constraints further comprise a set of constraints, and an order in which the set of constraints is applied is dependent upon the characterization of the failure.

11. The verification system of claim 10 wherein not every constraint within the set of constraints is applied to the characterization of the failure.

12. The verification system of claim 1 wherein the one or more constraints are generated by any of the following comprising:

(a) creation of cutpoints in the representation of the first design and the representation of the second design;

(b) input signals external to the representation of the first design and the representation of the second design; or

(c) state-holding elements contained within the representation of the first design and the representation of the second design.

13. A method of verifying functional similarity between a first design and a second design intended to satisfy functionality of the first design, comprising:

receiving a representation of the first design;

receiving a representation of the second design;

receiving a plurality of design inputs;

executing a test program on a computer that compares the representation of the second design with the representation of the first design, and detecting when the representation of the second design does not satisfy the representation of the first design, the test program providing a failure indicator and a characterization of a failure in response to the detecting, the test program further comprising:

applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and analyzing the failure by determining whether the one or more constraints will prevent the failure from occurring.

14. The method of claim 13 further comprising:

affirming that the second design is fully functionally equivalent to the first design.

15. The method of claim 13 further comprising:

obtaining the one or more constraints that are applied to the characterization of the failure as a portion of the plurality of design inputs that are received.

16. The method of claim 13 further comprising:

permitting another design separate from the first design and the second design to at least partially determine the one or more constraints.

17. The method of claim 13 further comprising:

creating a set of constraints, and applying predetermined ones of the set of constraints in an order that is dependent upon the characterization of the failure.

18. The method of claim 13 further comprising:

generating the one or more constraints by having constraints associated with any of the following comprising:

cutpoints created in the representation of the first design and the representation of the second design, input signals external to the representation of the first design and the representation of the second design, or state-holding elements contained within the representation of the first design and the representation of the second design.

19. A computer readable storage medium for storing a verification system, comprising:

a set of instructions, the set of instructions when executed implementing a verification process comprising:

receiving a representation of a first design representing a specification having a predetermined functionality;

receiving a representation of a second design, the representation of the second design intended to satisfy the predetermined functionality of the first design, the verification system functioning to affirm that the representation of the second design does in fact satisfy the predetermined functionality of the representation of the first design;

receiving a plurality of design inputs;

comparing the representation of the second design with the representation of the first design, and detecting when the representation of the second design does not satisfy the representation of the first design, the detecting resulting in providing a failure indicator and a characterization of a failure; and

applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring.

20. The computer readable storage medium of claim 19 further comprising:

maintaining the one or more constraints in a list that is applied in an order based upon the characterization of the failure in response to the set of instructions.

21. A verification system, comprising:

a representation of a first design representing a specification having a predetermined functionality;

a representation of a second design, the representation of the second design intended to satisfy the predetermined functionality of the first design, the verification system functioning to affirm that the representation of the second design does in fact satisfy the predetermined functionality of the representation of the first design;

a plurality of design inputs;

a tester for comparing the representation of the second design with the representation of the first design, and detecting when the representation of the second design does not satisfy the representation of the first design, the tester providing a failure indicator and a characterization of a failure in response to the detecting, the tester further comprising:

a symbolic stimulus generator that analyzes the representation of the first design to determine a set of inputs to a test point and generates a set of symbolic stimulus to be applied to corresponding test point inputs in the

representation of the second design, the tester accepting as an additional input one or more additional nodes in the first design, finding additional inputs corresponding to the additional nodes, generating a second set of symbolic stimulus from the additional inputs, applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design, and generating an output response for use in verifying functional similarity.

22. The verification system of claim 21 wherein the finding of additional inputs corresponding to the additional nodes comprises tracing from an output-to-input direction through the representation of the first design to identify the additional inputs.

23. The verification system of claim 21 wherein the corresponding inputs in the representation of the second design do not structurally exist in identical form in the representation of the first design, but correspondence in functional result exists.

24. A method of verifying functional similarity between a first design and a second design intended to satisfy functionality of the first design, comprising:

receiving a representation of the first design;

receiving a representation of the second design;

receiving a plurality of design inputs;

comparing the representation of the second design with the representation of the first design, detecting when the representation of the second design does

not satisfy the representation of the first design, and providing a failure indicator and a characterization of a failure in response to the detecting;

analyzing with a symbolic stimulus generator the representation of the first design to determine a set of inputs to a test point;

generating a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design;

accepting as an additional input one or more additional nodes in the first design;

finding additional inputs in the first design corresponding to the additional nodes;

generating a second set of symbolic stimulus from the additional inputs; and

applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design and generating an output response for use in verifying functional similarity.

25. The method of claim 24 wherein the finding additional inputs in the first design corresponding to the additional nodes further comprises tracing from an output-to-input direction through the representation of the first design to identify the additional inputs.

26. A computer readable storage medium for storing a verification system, comprising:

a set of instructions, the set of instructions when executed implementing a verification process comprising:

receiving a representation of the first design;

receiving a representation of the second design;

receiving a plurality of design inputs;

comparing the representation of the second design with the representation of the first design, detecting when the representation of the second design does not satisfy the representation of the first design, and providing a failure indicator and a characterization of a failure in response to the detecting;

analyzing with a symbolic stimulus generator the representation of the first design to determine a set of inputs to a test point;

generating a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design;

accepting as an additional input one or more additional nodes in the first design;

finding additional inputs in the first design corresponding to the additional nodes;

generating a second set of symbolic stimulus from the additional inputs; and

applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design and generating an output response for use in verifying functional similarity.